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Which Way For 16K?

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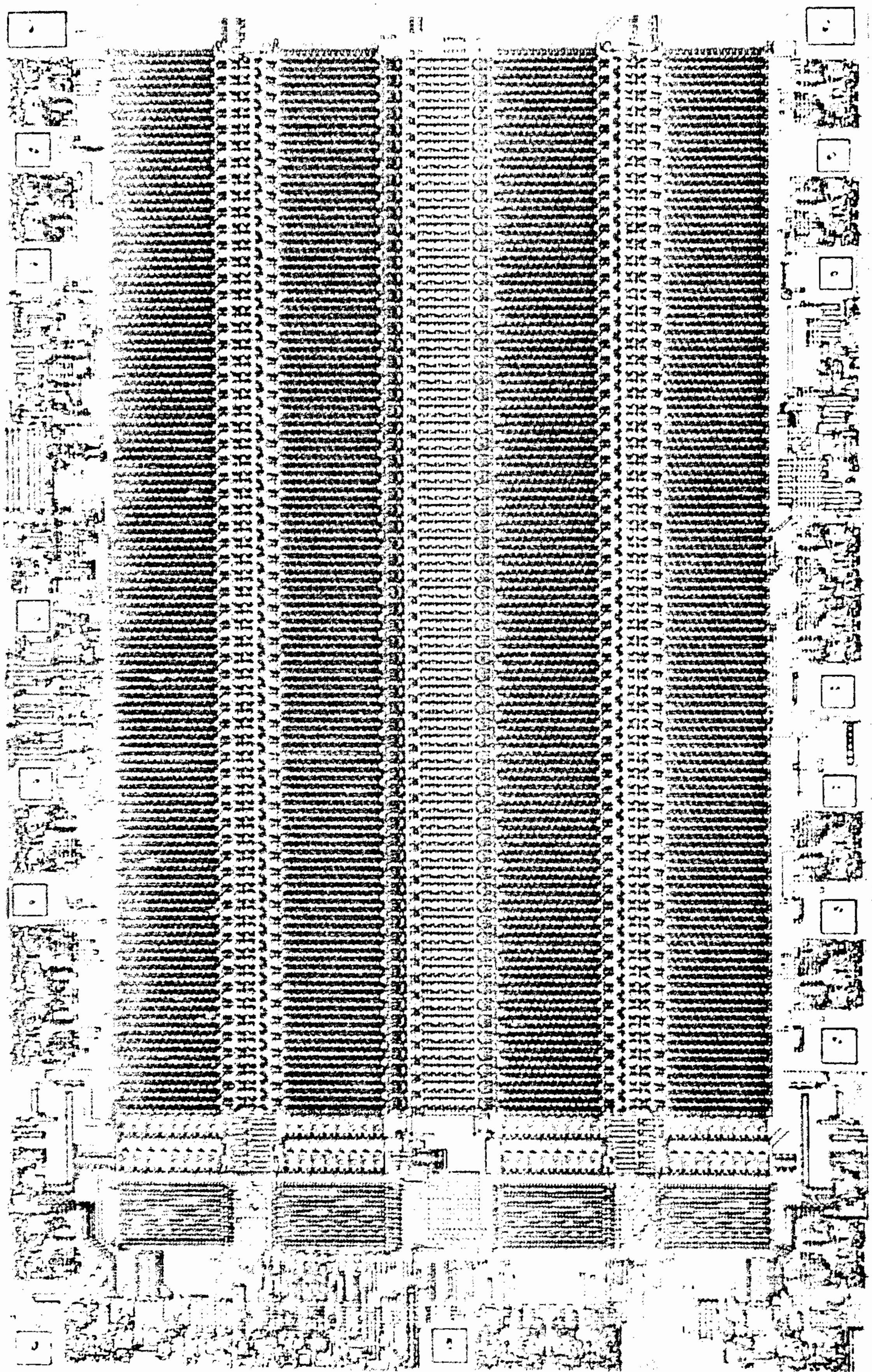


WHICH WAY FOR 16K?

The engineers who struggled through the pin-out confusion (16, 18 or 22 pin) on the 4K Random Access Memories (RAMs) and very adamantly protested the lack of pinout standardization among manufacturers have gotten their wish with the 16K RAMs, almost.

The 16K RAMs are all in 16-pin packages, have the same pinout, are TTL compatible, with multiplexed addresses, two clocks, and basic operation like the 16-pin 4K RAMs. There are differences with respect to refresh modes and data output operation but these variations do not preclude a system design which will accept all of the devices.

A FRESH APPROACH TO REFRESH

One of the most requested features Intel encountered during the market research efforts that led to the 2116 definition was the ability to refresh the data cell matrix with only 64 cycles. With this in mind, Intel implemented the 2116 in such a manner that both 64 cycle and 128 cycle refresh modes are available and the user has the option as to which mode best suits his system needs. Figure 1 shows that the 2116 is really two 8K x 1-bit RAMs sharing some common circuits. In normal data operations (Read, Write, etc.) the seventh address bit, A_6, is decoded and selects only one 8K half to be powered up during any given cycle.

64-Cycle Mode

The $\overline{CAS}$-before-$\overline{RAS}$ 64 cycle refresh mode operates by disabling the common I/O circuitry shown in Figure 1a and refreshing one row in both 8K x 1-bit halves of the 2116. Since there are 64 rows in each 8K half and one row in each half is refreshed each cycle, only 64 refresh cycles are required.

128-Cycle Modes

During Read/Refresh and $\overline{RAS}$-only refresh cycles, only one 8K x 1-bit half of the 2116 is activated and one of the 64 rows in the active section is refreshed. Thus 128 cycles are required to refresh the 128 rows of cells (64 rows in each half of the RAM).

EFFECTS OF REFRESH

The requirement for refreshing the data stored in the cells of a 16K dynamic RAM such as the 2116 impacts system characteristics in three areas; memory available time or throughput, system standby power, and the maximum usable page size during page mode operation. The 64 cycle refresh mode of the 2116 offers improved performance in all these areas over the 128 cycle refresh mode.

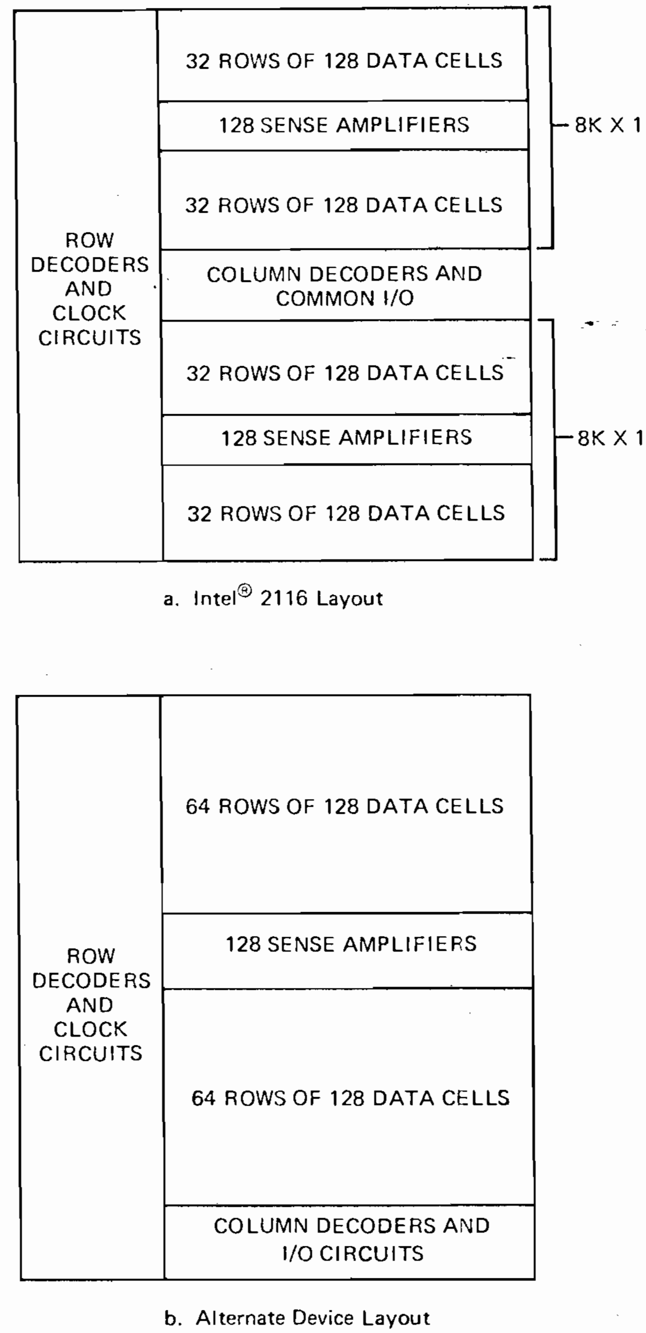


Figure 1. 16K RAM Device Configurations

Memory Availability

Assuming a minimum cycle time of 375 nsec, 128 refresh cycles in 2 msec requires 48 μsec or 2.4% of the available memory time. But that's a minimum. Typical computer memory cycle times run closer to 700-900 nsec, so 128 cycle refresh typically requires 102 μsec or 5.1% of the available memory time. 64 cycle refresh requires only 51 μsec or 2.5% of the available memory time under the same conditions of 700-900 nsec cycle time. (See Table I). That's higher throughput capability and less chance of having to wait for completion of a refresh cycle to start a data access.

Table I. Time Impact Of Refresh

Refresh Mode	System Cycle Time	Requirements of Refresh: Time Spent On Refresh During Each 2 msec	Requirements of Refresh: Percent Of Available Memory Time
64 cycle	375 nsec	24 μsec	1.2%
	800 nsec	51 μsec	2.6%
128 cycle	375 nsec	48 μsec	2.4%
	800 nsec	102 μsec	5.1%

System Standby Power

Remember, the 2116 can be refreshed each 2 milliseconds in one of three ways; 128 Read cycles, 128 $\overline{RAS}$-only cycles, or 64 $\overline{CAS}$-before-$\overline{RAS}$ cycles. The standby power (refresh only) for the three types of 2116 refresh cycles is given in Table II.

Table II. Power Considerations For Refresh

Parameter \ Cycle	Read/ Refresh	$\overline{RAS}$-Only Refresh	$\overline{CAS}$-Before-$\overline{RAS}$ Refresh
Refresh Cycles	128	128	64
Power Per 500 nsec Cycle	444 mW	346 mW	426 mW
Average Refresh Power	31 mW	28 mW	24 mW

"Wait a minute," you say! "If you turn on both 8K x 1-bit halves of the 2116 during 64 cycle refresh, why is the power per cycle less than during a Read/Refresh cycle and why is the average power less than with either Read/Refresh or $\overline{RAS}$-only cycles?" Let's take these questions one at a time!

The *per cycle* power with $\overline{CAS}$-before-$\overline{RAS}$ is lower than for the Read/Refresh cycles because the $\overline{CAS}$ clock generator circuits and column decoders do not operate during 64 cycle refresh and the common I/O circuits are off. The power reduction due to these circuits being off more than offsets the increase in power dissipation due to both halves of the RAM being on.

The *average power* is lower with $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles because there are only 64 cycles each 2 milliseconds rather than 128. The 2116 is, therefore, in standby a larger percentage of time during the 2 millisecond refresh period. Although the $\overline{CAS}$-before-$\overline{RAS}$ *per cycle* power is 23% higher than the $\overline{RAS}$-only per cycle power, the *average* power is 14% lower!

There is one other power related characteristic of $\overline{CAS}$-before-$\overline{RAS}$ refresh which must be considered. The peak value of the transient currents during a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle is approximately 20% higher than during the other two refresh modes. This is caused by the capacitive charging/discharge currents associated with 128 additional sense amplifiers. Care must be taken in the system design to decouple the slightly higher transient peaks. Work in the Intel Applications Lab has shown that the decoupling and board layout suggestions included in the 2116 data sheet yield acceptable power distribution noise levels with any of the allowable refresh modes.

Refresh-Page Mode Interaction

Page mode operation with 16K RAMs allows faster successive memory data operations at the 128 *column* locations in a single addressed *row*. Receipt of a $\overline{RAS}$ and a 7-bit row address byte causes the RAM to access the 128 data cells c the addressed row.

At access time all 128 data bits are available at the sense amplifier outputs as long as $\overline{RAS}$ is held active. By cycling the $\overline{CAS}$ clock and addressing the desired data bit with the 7-bit column address byte all 128 data bits may be brought to the data output of the device. Data access and cycle time in this mode, called page mode, is faster than normal data cycles. Page mode is an excellent way to transfer blocks of data to and from memory at high speed, but it is impacted by refreshing. The refresh requirements of the devices limit the number of consecutive page mode cycles to less than the 128 available from each row of devices. As an example, recall that the 2 millisecond distributed refresh mode requires a refresh cycle every 15.5 microseconds, (for 128 cycle refresh mode) and every 31 microseconds (for the 2116 in its 64 cycle refresh mode). This means that the devices may remain in the page mode for a period no longer than the time required between refresh cycles.

For example, for systems using 128 cycle refresh, the maximum time in the page mode is 15.5 μsec. For systems using 64 cycle refresh the time in page mode is doubled to 31 μsec. In practice, this limits the number of consecutive page mode cycles to 55 or less for the designs which use 128 refresh cycles and to 110 or less for the 2116 in its 64 cycle refresh mode. The 2116 with its 64 cycle refresh mode clearly permits more useful page mode operation than would a 16K RAM which requires 128 refresh cycles. Table III summarizes the impact of refresh upon page mode operation.

Table III. Refresh Impact Upon Page Mode Operation

Refresh Mode	Time Period Between Refresh Cycles	Number of Page Mode Cycles Possible Between Refresh Cycles
128 Cycle/2msec Read, or $\overline{RAS}$ - Only	15.5 μsec	55
64 Cycle/2msec 2116 $\overline{CAS}/\overline{RAS}$ mode	31.0 μsec	110

IMPLEMENTATION OF 64/128 CYCLE REFRESH MODES

Provision for 64 cycle refresh was a major factor in the selection of the device architecture shown in Figure 1a for the 2116. There are, however, several other performance and yield related advantages to the 2116 architecture.

Implementing 64 cycle refresh requires limiting the number of data cells per sense amplifier to 64. That means 256 sense amplifiers are required (16,384 cells ÷ 64 cells/sense amp=256 sense amps). 128 cycle refresh would force 128 cells per sense amplifier and only 128 sense amplifiers. So the question boils down to a 256 x 64-bit organization versus a 128 x 128-bit organization. (See Figure 1).

256 Sense Amps Means Twice As Much Chip Area For Sense Amps

True, when you double the number of sense amps, you double the chip area required for sense amps. However, the sense amp area on the 2116 amounts to only 12% of the total chip area so reducing the number of sense amps to 128 would only reduce the chip area by 6% which isn't very significant.

128 Cells Per Sense Amplifier Means Larger Cells

Putting 128 storage cells on each sense amplifier would require the bit sense lines to be twice as long as with 64 cells per sense amp. This means the bit sense line capacitance would nearly double. To keep the sensed signal level the same, the cell-capacitance-to-bit-line-capacitance ratio must remain the same.

With double the bit sense line capacitance, the cell capacitance must be doubled and this would increase the chip area devoted to the storage cell by approximately 25%.

The cell capacitor could be made larger by less than a factor of two, but the signal-to-noise ratio of the sensing function would be degraded. It also would adversely affect the access time and device operating margins and is not a good alternative.

Complete Capatibility

The 128 cycle refresh mode offered with the 2116 is 100% compatible with other 16K RAMs that offer *only* 128 cycle refresh. That means that the 2116 fits into sockets designed for 64 cycle refresh *and* into sockets designed for 128 cycle refresh. Other RAMs only fit into sockets designed for 128 cycle refresh.

TO LATCH OR NOT TO LATCH

One area of non-compatibility between the announced 16K RAMs is the inclusion of an output latch on the device. This has given rise to a LATCHED/NON-LATCHED device debate. Let's examine the issue to understand the system effects of the output latch.

4K Compatibility

The 16-pin 4K RAM, available from a multitude of suppliers, established the standard for latched output, multiplexed address RAMs. All available 16-pin 4K RAMs have compatible latched outputs.

Since the 16-pin 16K is virtually identical to the 16-pin 4K in terms of pin-out and timing, it seems reasonable to make the interface between the two devices as close as possible. The 2116 is *fully* output compatible with *all* 16-pin 4K RAMs. This allows the unprecedented "luxury" to system designers of upgrading their system densities by a factor of four with only an address strapping change on their memory boards.

Also, no new learning curve is required for the system designers since the parts would operate the same. Chip select, $\overline{CS}$ (pin 13), on the 4K was actually latched and implemented as an address bit just like the 6 column address bits. Pin 13 on the 16K is address bit A_7.

A number of Intel's 16-pin 4K customers are using their 4K RAM boards to evaluate the 2116 with pin 13 jumpered to an address driver rather than the old $\overline{CS}$ driver. Even the test procedures can be the same.

Common I/O Operation

When designing with microprocessors that employ bi-directional I/O buses, the ability to connect memory devices directly to the bus can be an asset. A memory device without an output data latch can have it's Data-In and Data-Out pins connected together and directly to the I/O bus if the operation of the RAM is restricted to simple read and write cycles. Let's look at what this means in two separate classes of microprocessor systems.

Single Board Systems

Small microprocessor systems typically use a limited number of LSI circuits designed as a CPU-I/O combination and sold together as a chip set. Because of the limited number of devices connected to the microprocessor I/O bus, memory devices can often be directly connected to the data ports without any buffering or isolation devices. Since the bus is generally local to the chip set, and does not leave the printed circuit board, it is not subject to the risks of backplane voltage shorts and potential device destruction. These systems can benefit from direct RAM connection to the I/O bus. Single board microprocessor systems that employ bidirectional I/O buses can benefit from non-latched output RAMs because the Data-In and Data-Out pins can be tied together. These small systems use small amounts of memory, however, and it is often contained on the CPU chip or integrated into an I/O device. The amount of external RAM memory, when used, seldom exceeds 1K to 2K words and the 16K RAM will not find much usage in these small systems.

Multiple Board Systems

Larger microprocessor systems place the main RAM storage, or an expansion to the RAM storage, on separate printed circuit boards. All signals to and from the memory must then be buffered to prevent overloading of the microprocessor I/O bus and to protect the outputs (and inputs) of both the microprocessor and memory devices from accidental shorting to a supply voltage or to ground during troubleshooting and normal system maintenance/repair. The effect of these buffers (see Figure 2) is to eliminate any need or advantage to tying the RAM data input and output together.

It is in these larger systems that the 4K and 16K RAMs are most useful due to the size of the memory required. These systems normally use 12K to 64K bytes of memory and the density of the 16-pin RAMs is an asset. Common I/O RAM operation is not a factor in these systems. Besides, if common I/O is so important for RAMs in microprocessor systems, why does the RAM that is the most widely used in microprocessor systems today (the 2102) have separate I/O?

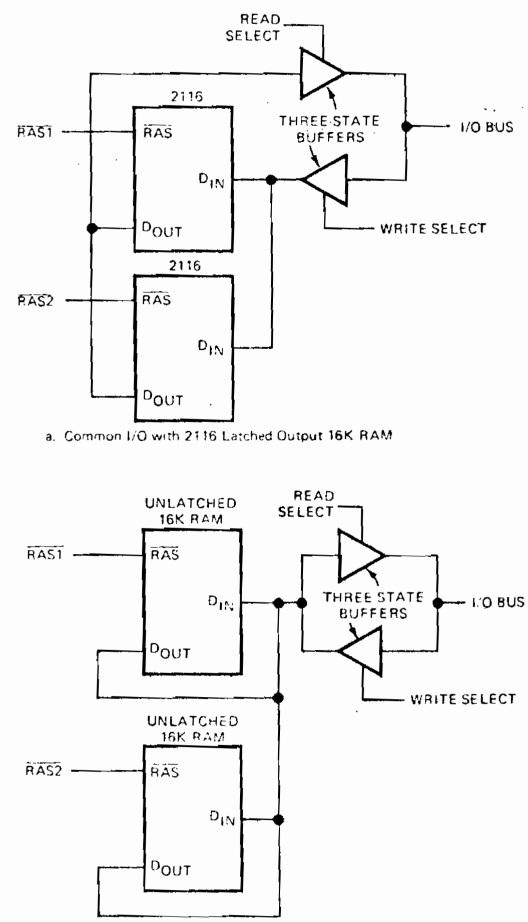
ADVANTAGES OF THE LATCH

There are a number of system advantages to the data-out latch on board the RAM. Some of the more important of these advantages are:

1) Many small, non-microprocessor systems, especially those which run with long system cycle times (1 μsec or more) need the data read from memory to be latched in order to minimize the clock or active time and minimize power dissipation. In these systems, the on-chip data latch is an asset because off-chip data latches increase the system power dissipation. Power dissipation for TTL data latches runs about 70 mW per bit. For 16K by 8-bit memory that is 70 mW per 16K and is a constant DC power drain during active or standby cycles. The on-chip latch adds only 24mW to the device power dissipation and only while the data output is active, not during standby.

2) Off chip latches require more packages on the memory board. A 16-bit system will require four 16 pin packages or two 24 pin packages. These latches take up board space and add part, assembly, and maintenance costs to the system.

3) Off chip latches also add to access time. The delay of an on chip latch is included in the access time for the device. Using an unlatched output device and adding external



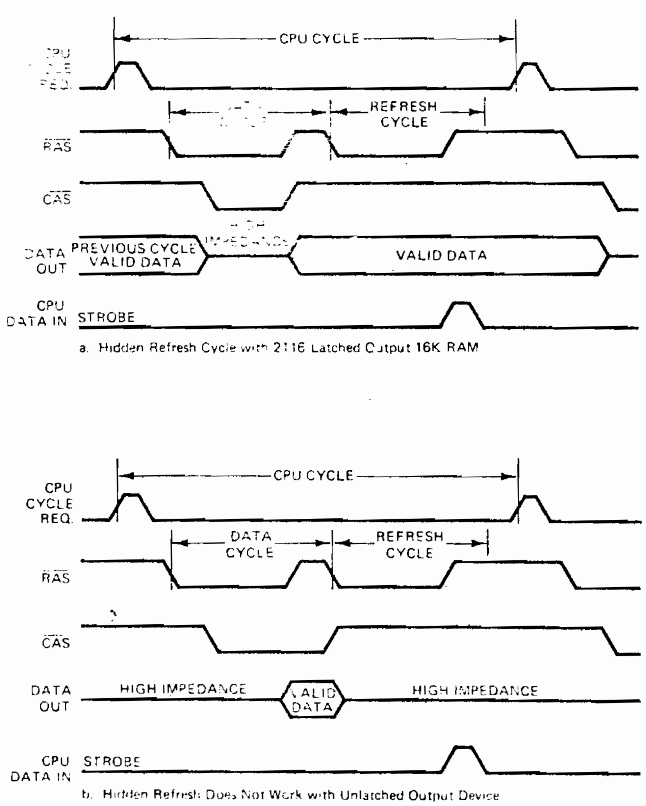
a. Common I/O with 2116 Latched Output 16K RAM

b. Common I/O With Typical Unlatched Output 16K RAM

Figure 2. Common I/O Configurations

latches adds typically about 20 nsec to system access time due to timing skew in the latch clock plus the latch propagation delay.

4) An operational feature that is offered in latched output RAMs and is not available on unlatched output RAMs is the ability to perform a refresh cycle immediately following a data cycle without impacting the availability of output data. This "hidden" refresh cycle is possible with the latched output device because a $\overline{\text{RAS}}$-only refresh cycle does not affect the data contained in the output latch. A typical timing diagram for the hidden refresh mode is shown in Figure 3. This mode of operation is not possible with the unlatched output devices unless external latches are added because the data output of the unlatched devices goes to the high impedance state at the beginning of the $\overline{\text{RAS}}$-only refresh cycle and is not available to the processor when required. This hidden refresh cycle feature of the 2116 and the latched output 4K RAMs can be used to advantage in many systems.



a. Hidden Refresh Cycle with 2116 Latched Output 16K RAM

b. Hidden Refresh Does Not Work with Unlatched Output Device

Figure 3. Hidden Refresh Cycle Operation

DISADVANTAGES OF THE LATCH

There are also a number of potential system disadvantages to the data out latch. These disadvantages are generally not practical limitations on system design due to other overriding considerations as discussed below:

1) Systems designed with latched 16K's whose outputs are OR-tied must provide $\overline{\text{CAS}}$ to every device during every cycle in order to deselect devices selected on the previous cycle. Although non-latched devices can and do operate in this mode, this $\overline{\text{CAS}}$ deselect cycle is not required and $\overline{\text{CAS}}$ can be decoded and sent to the selected devices only.

   Since $\overline{\text{CAS}}$ occurs after $\overline{\text{RAS}}$ in a cycle, a cycle could be started with $\overline{\text{RAS}}$ to every device and $\overline{\text{CAS}}$ decoded during t_{RCL} and applied only to the desired devices. Thus $\overline{\text{CAS}}$ is now like $\overline{\text{CS}}$ on the 16-pin 4K RAMs. This operation reduces access times by 10ns when using a 74S138 decoder since the chip select decode time is not required prior to $\overline{\text{RAS}}$ as it is with the latched output 16K RAMs. The practical usefulness of this operational mode is limited since using $\overline{\text{CAS}}$ as a chip select means that the unselected devices in a system dissipate power at a level only slightly less than the selected devices (See Table II $\overline{\text{RAS}}$-only cycle power). This mode dissipates almost as much power as that dissipated when using $\overline{\text{CS}}$ in 4K RAMs for deselection. (Which explains why nobody used $\overline{\text{CS}}$ for device selection with the 4K).

2) The Data-In and Data-Out pins may not be directly tied together and to a common I/O bus. This is a disadvantage only in single-board microprocessor systems and not in larger systems (refer to Figure 2).

WHICH NON-LATCHED 16K?

All non-latched 16K's are not alike! In fact, none of them are alike. The three currently released designs all react differently during either read or write cycles.

Data Output Control

The data output is controlled by $\overline{\text{CAS}}$ in both the latched and non-latched devices and becomes valid at column access time (t_{CAC}) after $\overline{\text{CAS}}$ goes low (active). The difference lies at the point in time at which the data out goes to the off (high-impedance) state. In the latched output case, data out goes to the off state after $\overline{\text{CAS}}$ goes low in the *next cycle*. In the non-latched output case, data out goes to the off state after $\overline{\text{CAS}}$ goes high in the *current* cycle.

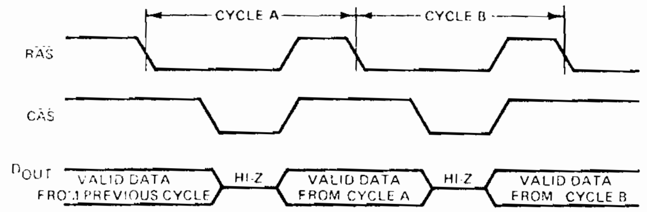


Figure 4. 2116 Data Output Operation

Unlatched Device Output Characteristics

Differences in characteristics of the outputs of non-latched devices are shown in Figure 5 for a read cycle.

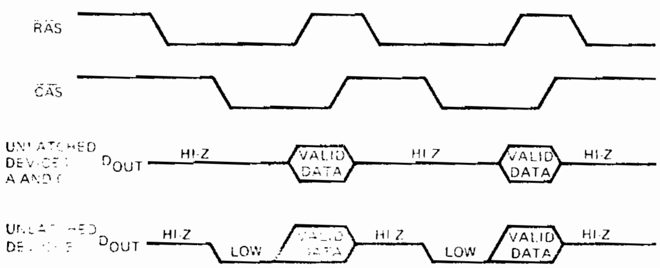


Figure 5. Unlatched Device Output Operation During Read Cycles

When it comes to a write cycle the data-out characteristics of the 3 suppliers are different from each other (see Figure 6). So why would anyone care what the *output* is doing during a write cycle? Incoming test programs and device qualification testing must account for these differences. Also, since the device outputs are connected to an I/O bus of some sort, the designer must consider the output operational characteristics to assure compatibility with the bus.

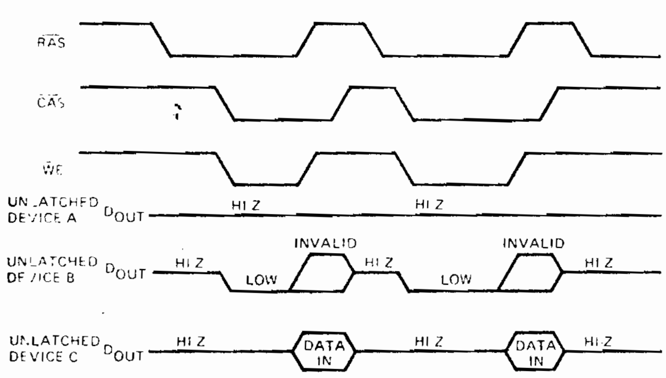


Figure 6. Unlatched Device Output Operation is Different During Write Cycles

None of the above differences by itself is hard to handle but it can be troublesome to have to account for all conditions especially in testing and qualifying the devices.

$\overline{\text{CAS}}$ AS A CHIP SELECT

During the discussion of the disadvantages of a data out latch, the use of $\overline{\text{CAS}}$ as a chip select signal was mentioned briefly. The system parameters affected by this use of $\overline{\text{CAS}}$ are access speed, power dissipation, and page mode.

Access Speed

Decoding the chip select address bits and gating $\overline{\text{CAS}}$ only to the selected devices reduces access times by about 10 nanoseconds compared to gating $\overline{\text{RAS}}$ as the chip select signal.

Power Dissipation

Using $\overline{\text{CAS}}$ as the chip select signal means that the unselected devices in a system dissipate $\overline{\text{RAS}}$-only power levels while the selected devices dissipate full power levels.

What does that mean in a 128K x 8-bit system? Decoding only $\overline{\text{CAS}}$ and supplying $\overline{\text{RAS}}$ to all 64 devices means one row of devices would dissipate normal power while seven rows would dissipate $\overline{\text{RAS}}$-only power levels during each cycle. The 128K by 8-bit system (8 rows of 16 devices) will dissipate 23.0 Watts in this mode.

Decoding only $\overline{\text{RAS}}$ as chip select and supplying $\overline{\text{CAS}}$ to every device does add slightly to access time (about 10 nsec) but it also means only 8 devices of the 64 in our example system would be active in any given cycle while the other 56 devices would remain in refresh/standby. The same 128K x 8-bit system will dissipate 5.2 Watts in this mode. (See Table IV).

Table IV. Power Considerations for 128K x 8-bit System

Operational Mode / System Parameter	Decoded $\overline{\text{RAS}}$	Decoded $\overline{\text{CAS}}$
I_{DD} Current	0.43 Amps	1.92 Amps
Power Dissipation	5.2 Watts	23.0 Watts

Page Mode

In the non-latched RAM, $\overline{\text{CAS}}$ used as a chip select signal allows extension of the page mode boundary beyond 128 data cells. This is accomplished by supplying $\overline{\text{RAS}}$ to all the devices in a system and $\overline{\text{CAS}}$ to the selected devices extending the boundary to include the selected row in all of the RAMs in the system. This operation is valid but there are some practical restrictions on its usefulness.

Extension of the page mode boundary again requires activating all the devices in the system rather than just one row of devices. The increase in power dissipation incurred makes this mode of operation rather undesirable as previously discussed. In addition, the refresh requirements of the devices limits the number of consecutive page mode cycles to less than the 128 available from *one* row of *one* device. Remember that refresh requires $\overline{\text{RAS}}$ to be cycled to refresh a row of cells every 15.5 microseconds with the 128 refresh cycle mode and 31 microseconds with the 2116 in its $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ 64 cycle refresh mode. Why activate *all* of the RAMs in the system when you can't even cycle through all the locations in *one* row of *one* RAM in a single page mode cycle?

SUMMARY

The goals for the 2116 16K RAM, increased bit density while maintaining performance and functional compatibility with the 16-pin 4K RAMs, have been achieved. This compatibility is a boon to the users since no new learning curve is needed when upgrading to the 16K RAM.

While there are differences in the announced 16K RAMs, these differences are slight when compared to the differences between the proliferation of 4K RAMs. By including TTL data out latches in the board design and using 128 cycle refresh, the designer can accommodate any of the 16-pin 16K devices.

For those users who wish to maintain the throughput rate of the 4K devices, the 64 cycle refresh mode of the Intel 2116 is ideal. The on board data out latch of the 2116 is a definite asset to those users with restrictive board space limitations. In extremely cost sensitive applications, the 2116's data out latch not only eliminates the need for external TTL latches but also reduces system power dissipation thereby reducing power supply and cooling costs.

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